TOSHIBA

INSULATED GATE BIPOLAR TRANSISTOR

MG15J6ES40

GTR Module

Silicon N Channel IGBT

High Power Switching Applications

Motor Control Applications

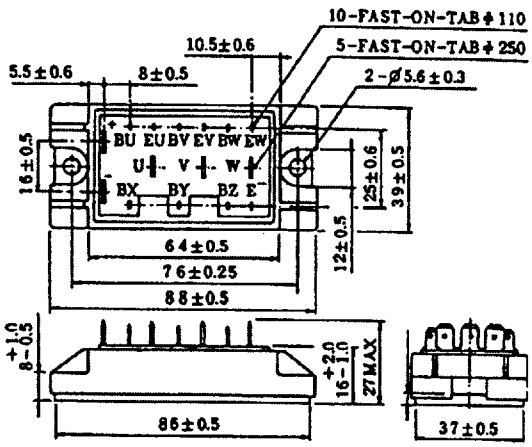
Features

- 6 IGBTs are built into 1 package
- High speed: t_f = 0.35μs (Max.) (I_C = 15A)
  t_{rr} = 0.15μs (Max.) (I_C = 15A)
- Low saturation voltage: $V_{CE\ (sat)}$ = 3.5V (Max.) (I_F = 15A)
- Enhancement mode
- The electrodes are isolated from case

Maximum Ratings (Tc = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Collector-Emitter Voltage		V_{CES}	600	V
Gate-Emitter Voltage		V_{GES}	± 20	V
Collector Current	DC	I_C	15	A
	1ms	I_{CP}	30	
Forward Current	DC	I_F	15	A
	1ms	I_{FM}	30	
Collector Power Dissipation		P_C	80	W
Junction Temperature		T_j	150	°C
Storage Temperature Range		T_{stg}	-40 ~ 125	°C
Isolation Voltage		V_{Isol}	2500 (AC 1 Minute)	V
Screw Torque		—	3	N ¥ m

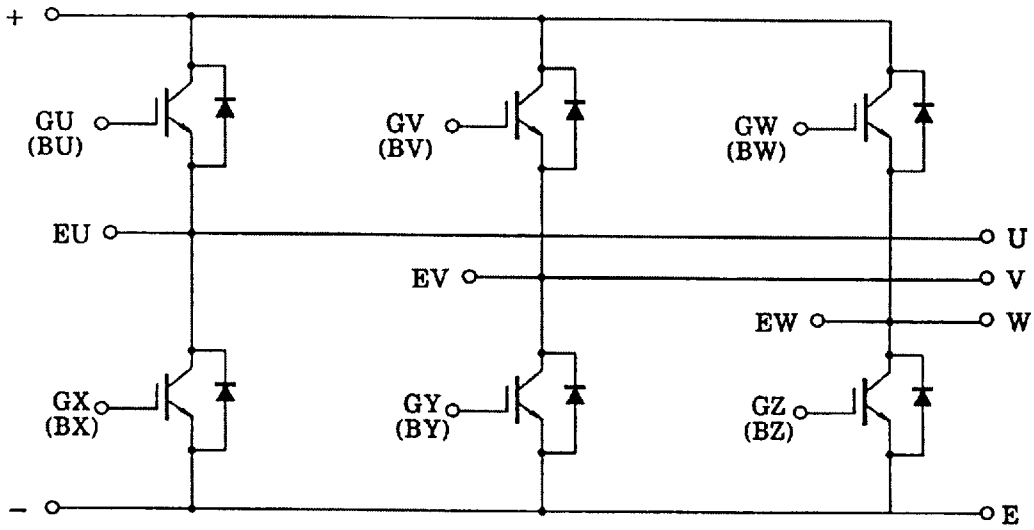
Unit in mm



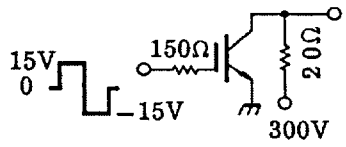
JEDEC	—
EIAJ	—
TOSHIBA	2-64A2A

Weight : 152g

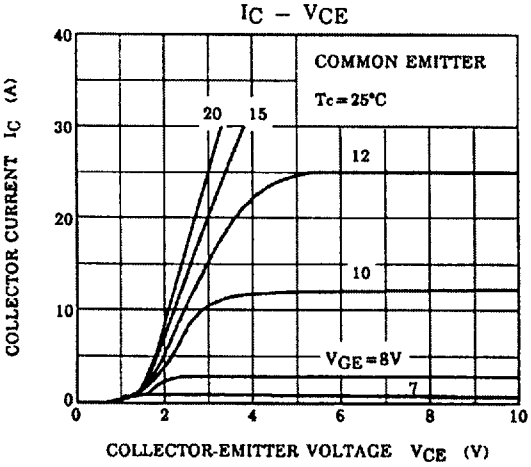
Equivalent Circuit



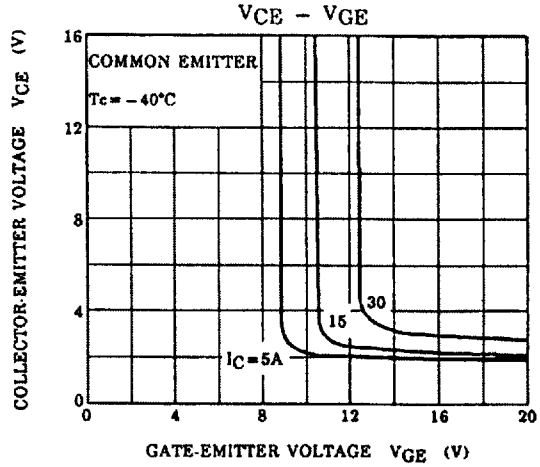
Electrical Characteristics (Tc = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Gate Leakage Current		I_{GES}	V_{GE} = ± 20V, V_{CE} = 0	—	—	± 500	nA
Collector Cut-off Current		I_{CES}	V_{CE} = 600V, V_{GE} = 0	—	—	1.0	mA
Collector-Emitter Breakdown Voltage		$V_{(BR)\ CES}$	I_C = 10mA, V_{GE} = 0	600	—	—	V
Gate-Emitter Cut-off Voltage		$V_{GE\ (OFF)}$	I_C = 15mA, V_{CE} = 5V	3.0	—	6.0	V
Collector-Emitter Saturation Voltage		$V_{CE\ (sat)}$	I_C = 15A, V_{GE} = 15V	—	2.7	3.5	V
Input Capacitance		C_{ies}	V_{CE} = 10V, V_{GE} = 0, f = 1MHz	—	1400	—	pF
Switching Time	Rise Time	t_r		—	0.30	0.60	µs
	Turn-on Time	t_{on}		—	0.40	0.80	
	Fall Time	t_f		—	0.18	0.35	
	Turn-off Time	t_{off}		—	0.60	1.00	
Forward Voltage		V_F	I_F = 15A, V_{GE} = 0	—	2.0	2.7	V
Reverse Recovery Time		t_{rr}	I_F = 15A, V_{GE} = -10V di/dt = 50A/µs	—	0.08	0.15	µs
Thermal Resistance		$R_{th\ (j-c)}$	Transistor	—	—	1.56	°C/W
			Diode	—	—	2.80	

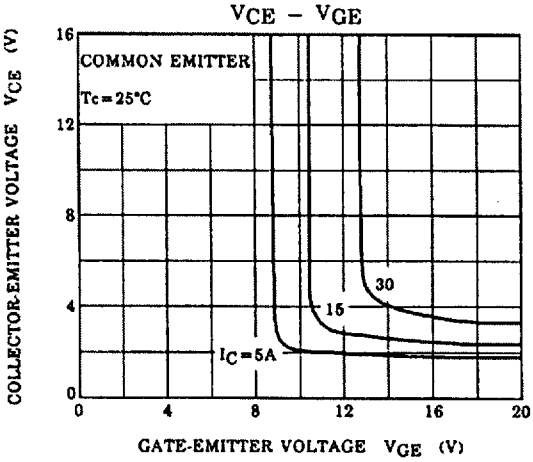
I_C – V_{CE}



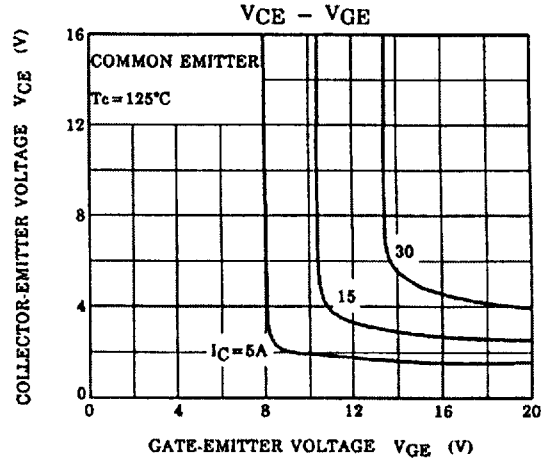
V_{CE} – V_{GE}



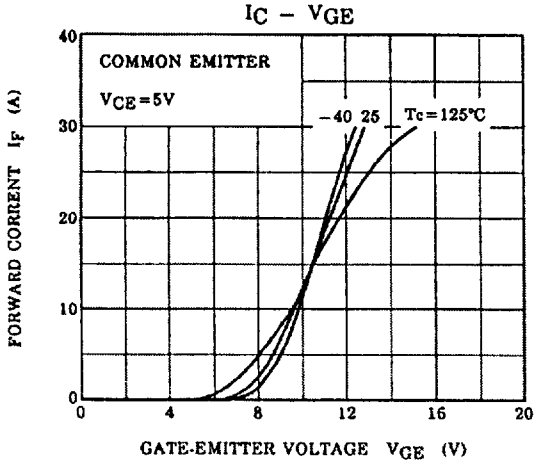
V_{CE} – V_{GE}



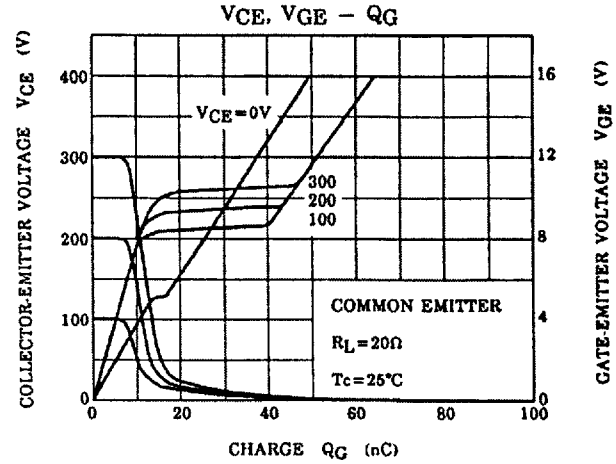
V_{CE} – V_{GE}



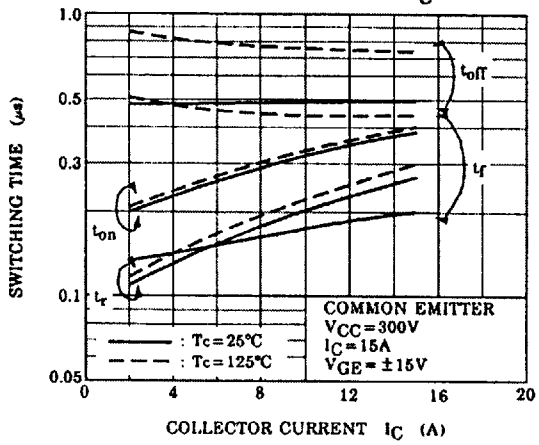
I_C – V_{GE}



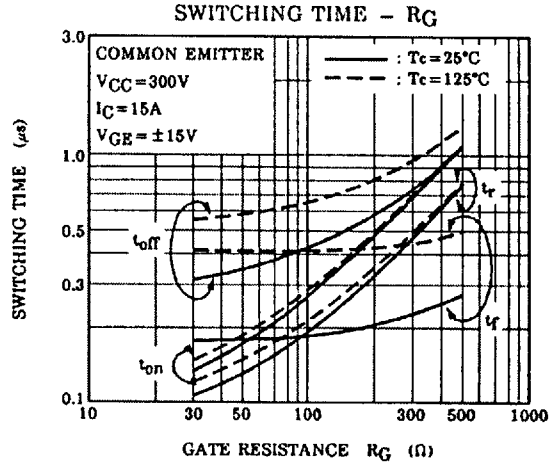
V_{CE}, V_{GE} – Q_G



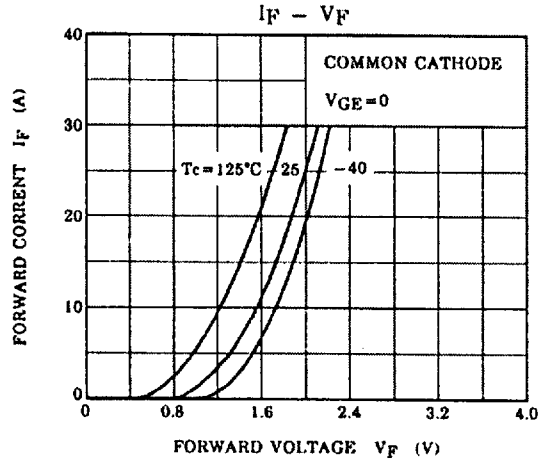
SWITCHING TIME – I_C



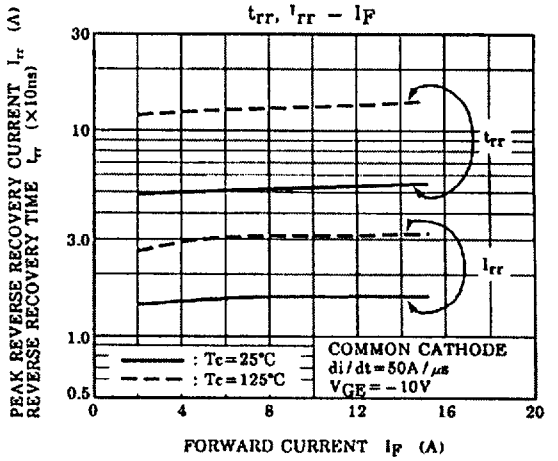
SWITCHING TIME – R_G



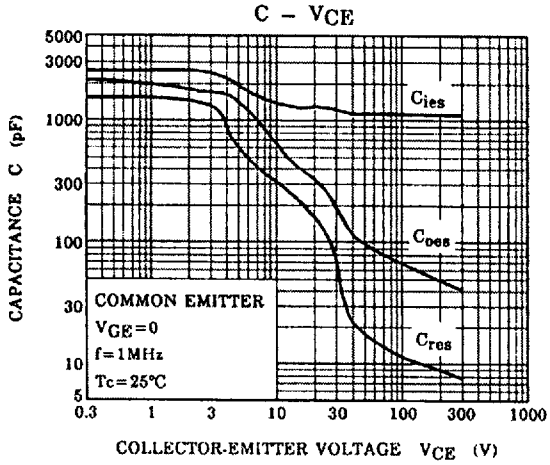
I_F – V_F



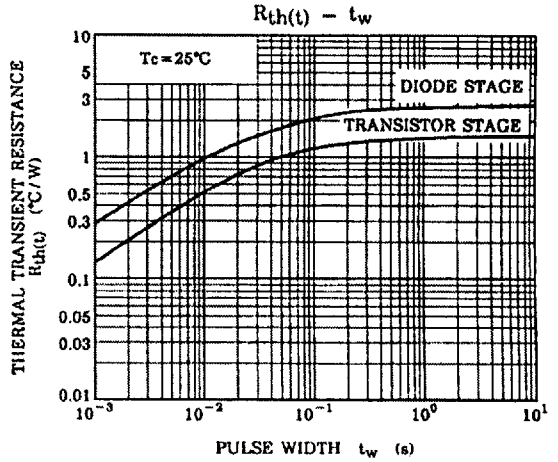
t_{rr}, I_{rr} – I_F



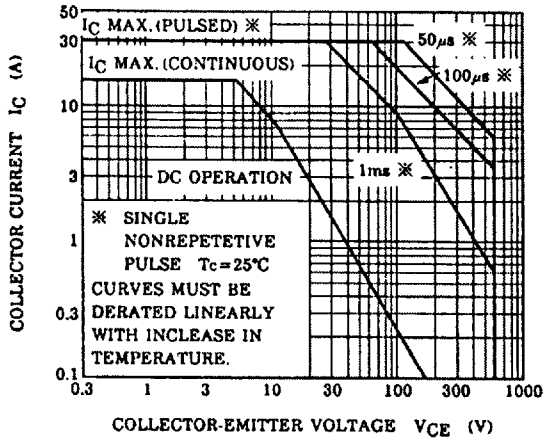
C – V_{CE}



$R_{th(t)}$ – t_w



SAFE OPERATING AREA



REVERSE BIAS SOA